AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method of generating an output clock signal from a phase-locked loop (PLL), the method comprising:

determining successive phase difference values between a reference clock signal and said output clock signal;

filtering said successive phase difference values to generate successive control values;

controlling a frequency of said output clock signal based on said successive control values; and

adapting a filter used to filter said successive phase difference values based on average control values determined from said successive control values.

2. (Original) The method of claim 1 further comprising detecting a trend in said average control values and determining a filter state based on said trend in said average control values.

3. (Original) The method of claim 2 further comprising selecting a fast filter setting for said filter when said trend indicates that said average control values have not stabilized.

4. (Original) The method of claim 2 further comprising selecting a slow filter setting for said filter when said trend indicates that said average control values have stabilized.

5. (Original) The method of claim 1 further comprising determining difference values between successive ones of said average control values, and wherein adapting said filter based on said average control values determined from said successive control values comprises adapting said filter based on processing said difference values.

6. (Original) The method of claim 5 wherein adapting said filter based on processing said difference values comprises:

integrating a number of said difference values to determine an integrated value of said number of said difference values; and

adapting said filter based on said integrated value.

7. (Original) The method of claim 6 wherein adapting said filter based on said integrated value comprises setting said filter to a slow filter state if said integrated value is below a defined threshold.

8. (Original) The method of claim 5 wherein adapting said filter based on processing said difference values comprises:

identifying peak values in said difference values; and

adapting said filter based on said peak values.

9. (Original) The method of claim 8 wherein adapting said filter based on said peak values comprises setting said filter to a slow filter state if a summation of a number of successive peak values is below a defined threshold.

10. (Original) A method of controlling a phase-locked loop (PLL) to reduce clock deviations in an output signal generated by the PLL relative to clock deviations in an input reference timing signal to the PLL, the method comprising:

generating a phase error signal by determining a phase difference between said input reference timing signal and said output signal;

filtering said phase error signal with a digital filter to produce a digital control value;

determining average control values by averaging successive ones of said digital control value; and

adapting a filter characteristic of said digital filter based on said average control values.

11. (Original) The method of claim 10 wherein adapting said filter characteristic of said digital filter based on said average control values comprises:

adapting said digital filter such that relatively heavy filtering is applied to said phase error signal when successive average control values indicate a locked condition of the PLL; and

adapting said digital filter such that relatively light filtering is applied to said phase error signal when successive average control values indicate an unlocked condition of the PLL.

12. (Original) The method of claim 10 wherein said digital filter is a proportional-integral (P-I) digital filter and adapting said filter characteristic of said digital filter based on the average control values comprises changing a value of a proportional digital filter coefficient K_p and an integral digital filter coefficient K_i.

13. (Original) The method of claim 10 wherein adapting said filter characteristic of said digital filter based on said average control values comprises:

determining difference values between successive ones of said average control values;

integrating said difference values to determine an integrated value; and

adapting said filter characteristic of said digital filter based on said integrated value.

14. (Original) The method of claim 13 wherein said adapting said filter characteristic of said digital filter based on said integrated value comprises changing from a relatively slow filter time constant to a relatively fast filter time constant if said integrated value is above a first integrated value threshold.

15. (Original) The method of claim 14 further comprising changing back to said relatively slow filter time constant if said integrated value falls below a second integrated value threshold.

16. (Original) The method of claim 15 further comprising changing back to said relatively slow filter time constant if said integrated value does not fall below said second integrated value threshold after a defined duration of time.

17. (Original) The method of claim 14 further comprising:

estimating a mean nominal value for said digital control value while PLL is operating with said relatively fast filter time constant; and

setting said digital control value to said mean nominal value.

18. (Original) The method of claim 13 further comprising entering a locked state of operation for said PLL if said integrated value is below a locked state integrated value threshold.

19. (Original) The method of claim 18 further comprising storing a long-term control value average for use during a subsequent initialization of said PLL if said integrated value remains below said locked state integrated value threshold for a defined duration.

20. (Original) The method of claim 13 further comprising:

estimating a trend of said digital control values;

calculating an estimated nominal value for said digital control value based on

determining an estimated trend minimum; and

setting said digital control value to said estimated nominal value.

21. (Original) The method of claim 13 further comprising:

identifying peak values in successive ones of said integrated value;

summing a number of peak values to determine a peak summation value; and

entering a locked state of operation for said PLL if said integrated value is below a

locked state peak value threshold.

22. (Original) The method of claim 13 wherein said adapting said filter characteristic of said digital filter based on said integrated value comprises changing from a relatively slow filter time constant to a relatively moderate filter time constant if said integrated value exceeds a locked state integrated value threshold.

23. (Original) The method of claim 22 further comprising changing from said relatively moderate filter time constant to said relatively slow filter time constant if said integrated value falls below an unlocked state integrated value threshold.

24. (Currently amended) A phase-locked loop comprising:

a controllable oscillator providing an output signal from the PLL at a frequency proportionate to an oscillator control signal;

a phase detector providing a phase error signal by detecting a phase difference between an input signal and said output signal;

an adjustable loop filter providing control values based on filtering said phase error signal;

a control circuit providing the oscillator control signal responsive to said control values; and

control logic to control a filter characteristic of said loop filter based on an average control value determined from successive ones of said control values to minimize clock deviations in said output signal.

25. (Original) The phase-locked loop of claim 24 wherein said control logic is operable in one of a defined number of states, and further wherein said control logic adjusts said filter characteristic of said loop filter based on a current state of said control logic.

26. (Original) The phase-locked loop of claim 25 wherein said control logic transitions from a first state to a second state based on at least one characteristic of said average control values.

27. (Original) The phase-locked loop of claim 26 wherein said control logic adjusts said filter characteristic of said loop filter based on a difference between successive average control values.

28. (Original) The phase-locked loop of claim 27 wherein said control logic further adjusts said filter characteristic of said loop filter based on a trend in said difference between successive average control values.

29. (Original) The phase-locked loop of claim 27 wherein said control logic further adjusts said filter characteristic of said loop filter based on an integration of said average control values.

30. (Original) The phase-locked loop of claim 24 wherein said phase detector comprises:

a first counter driven by clock transitions in said input signal and configured to generate a count overflow signal upon reaching a defined count;

a second counter driven by clock transitions in said output signal and configured to output a current count value;

a count register configured to capture said current count value of said second counter in response to said count overflow signal; and

processing logic adapted to determine said phase error signal based on differences in successive current count values.

31. (Original) The phase-locked loop of claim 30 wherein said processing logic comprises a portion of said control logic.

32. (Original) The phase-locked loop of claim 24 wherein said loop filter comprises a digital loop filter adapted to output said control value in a digital format.

33. (Original) The phase-locked loop of claim 32 wherein said digital loop filter is a proportional-integral (P-I) filter, and further wherein said control logic is adapted to update a proportional coefficient and an integral coefficient to effect changes in said at least one filter characteristic.

34. (Original) The phase-locked loop of claim 24 wherein said control circuit is a digital-to-analog converter (DAC), and further wherein said control value provided by said loop filter is a digital value conforming to an input range of said DAC such that said DAC generates a control voltage as said oscillator control signal relative to said digital value.

35. (Original) The phase-locked loop of claim 34 wherein said controllable oscillator is a voltage-controlled oscillator (VCO), and further wherein said VCO generates said output signal at a frequency determined by a value of said control voltage generated by said DAC.

36. (Original) The phase-locked loop of claim 34 wherein said control logic determines a DAC initial value based on said average control values and stores said DAC initial value in associated memory for loading into said DAC upon a subsequent initialization of said PLL.

37. (Original) The phase-locked loop of claim 24 wherein said control operates in one of a defined number of states, with each of said states corresponding to a desired filter setting for said loop filter, and to control transitions between said states based on processing average control values determined from said control values.

38. (Original) The phase-locked loop of claim 37 wherein said control logic controls said transitions between said states based on difference values determined from successive ones of said average control values.

39. (Original) The phase-locked loop of claim 24 wherein said control logic comprises a digital processor.